Multicore Test Based Built In Self-Test Architecture Using Majority Logic

D.Vanitha,
PG Scholar, Department of ECE, Nandha Engineering College, Erode-52, Tamilnadu, India.

Dr.S.Kavitha
Professor and Dean,Department of ECE, Nandha Engineering College, Erode-52, Tamilnadu, India.

Abstract – Embedded cores are now commonplace in large system-on-chip designs. However, since embedded cores are not directly accessible via chip inputs and outputs, special access mechanisms are required to test them at the system level. Test-access architecture, also referred to as a test-access mechanism (TAM), provides on-chip test data transport. Now days, multi core processor consists of more number of complex digital architecture. This architecture is used for many applications and to improve the application performance level. But it has some problem due to circuit complexity level. Existing work is to modify the test pattern generation logic using preselect logic function. The existing work is pseudorandom test patterns with desired toggling levels and enhanced fault coverage gradient compared with the design for testability based circuit test pattern generators. Proposed system is to design a multi core parallel testing architecture using majority logic technique. This technique is used to test all internal cores in parallel form. This work is to implement the test pattern creation and to apply the scan chain process. This process is to analysis the separate core internal architecture output result values. The proposed system is to improve the TAM system performance level and to reduce the power consumption level also. The proposed system is used to increase the test pattern generation process.

Index Terms – Test access mechanism (TAM), system-on-chip (SoC), automatic test pattern generation (ATPG), automatic test equipment (ATE), preselected toggling (PRESTO) and design for testability (DFT).

1. INTRODUCTION

System-on-a-chip can reduce manufacture cost and offer rapid system implementation. But the testing of SoC is a significant and serious challenge. In modular test, core test wrapper isolates an embedded core from its environment and test access mechanism which transports the test data from the SoC pins to core terminals. Test data volumes are growing especially for delay test as the VLSI complexity increases. Recently, there is a growing interest in test data compression of SoC testing.ATE delivers compressed test data and on-chip decompressors expand them into the actual test patterns which will be transported into scan chains. In recent years, SoC test compression schemes based on linear decompression which can provide higher compression ratios. Test cubes for each core are encoded separately using LFSR reseeding. Seed variables are then delivered fromATE channels to successive cores. However, performing decompression outside cores poses a larger TAM bandwidth for transporting uncompressed data. The proposed approach improves the encoding efficiency of linear decompressors. The main idea is that the cores tested simultaneously share part of free variables. Non-pivot free variables for one test cube of a core can be reused to encode test cubes of other cores with negligible impact. This avoids wastingof excess free variables and improves the compression ratio. In conventional architecture the total TAM width is partitioned with fixed width. Cores using the same TAM lines are tested sequentially while those using the different TAM lines can be tested in parallel. The number of free variables dependents on the number of care bits in a test cube. In EDT, the free variables are delivered via tester Channel. Thus, tester channels can be in their full capacity to transport necessary test data for a couple of initial test cubes. However encoding the remaining test cubes may not require so many inputs.Many system-on-chip integrated circuits today contain multiple hierarchy levels for both design and test. Hierarchy imposes constraints on the manner in which tests must be applied to “parent” cores and their “child” cores. We have two approaches for efficient testing of SoC with hierarchical cores. In first approach, the problem is solved by extending a conventional wrapper design; this leaves full flexibility for TAM optimization and test scheduling. The second approach is based on a modified wrapper design for parent cores that operates in two disjoint modes for testing of parent and child cores. This has an impact on the test architecture and corresponding schedule. The integration of a complete electronic system on a single chip is now commonplace. To simplify and speed up test generation and to enhance test reuse, modular testing of SoC is strongly advocated. In modular testing, all embedded cores are tested independently from each other. This approach is mandatory for embedded non-logic components. Modular testing consists of test access mechanisms and test wrappers. While a test wrapper is a thin shell around a core that forms the interface between the core and its SoC environment. It provides switching between

various modes of operation, such as normal (functional) mode, core-internal test mode, and core-external test mode.

2. LITERATURE SURVEY

[1] T.D. Ter Braak, S.T. Burgess, H. Hurskainen, H.G. Kerkhoff, Bermeulen, X. Zhang in 2010 proposed "On-Line Dependability Enhancement of Multiprocessor SoCs by Resource Management", a new approach towards dependable design of homogeneous MPSoCs has been proposed. First, the NoC dependability is functionally verified via embedded software. Then the Xentium processor tiles and associated embedded SRAMs are periodically verified via on-line self-testing techniques, by using a new IIP Dependability Manager. Faulty tiles are electronically bypassed and replaced by other Xentium resources via embedded resource manager software based on the DM results. This integrated approach enables fast electronic fault detection/diagnosis and repair, and hence a high MPSoC availability. The dependability application runs in parallel with the actual GNNS application, resulting in a very dependable MPSoC. All parts have been verified by simulation.

[2] Saeed Shamshiri and Kwang-Ting Cheng in 2009 proposed "Yield and Cost Analysis of a Reliable NoC" The yield and cost of a multi-core chip improve significantly through the addition of some spare cores in the system. It provides an analytical model that covers not only cores but also routers and interconnects. In this model, for different chip components such as cores, level 1 and 2 caches, network interfaces, routers, and wires, consider parameters such as the raw yield, defect density, defect coverage of manufacturing test, shape and scale parameter of the failure rate curve, and defect coverage for the faults that happen in the field. These parameters may have different values for different components depending on the testing strategy used. Taking these parameters as input variables, are general and robust enough to handle a wide variety of NoC-based multi-core chips with different architectures including heterogeneous designs. Analysis supports multi-core chips which employ different approaches for reliable data transfer. The focus of this work is the effects of spare cores and wires on the total yield and cost of the system. In an on-chip network, roughly 80% of the faults are transient. Different fault tolerance approaches such as Forward Error Control (FEC), Automatic Repeat Query (ARQ) and multi-path routing have been used and compared in literature for reliable on-chip transmission. Permanent faults on wires occur during manufacturing or in the field and may cause the system to fail. Such system failures increase the manufacturing cost if they happen before shipment or else will cause a huge service cost if they happen in the field. This extra cost can be avoided by adding some spare wires to replace the permanently faulty wires before and after shipment.

[3] K. Zarb-Adami, A. Faulkner, J.G. Bij de Vaate, G.W. Kant and P.Picard in 2010 proposed "Beamforming Techniques for Large-N Aperture Arrays" Beam forming is central to the processing function of all phased arrays and becomes particularly challenging with a large number of antenna element (e.g.>100,000). The most appropriate beam forming technology will change over time due to semiconductor and processing developments and a hierarchical structure which is technology agnostic and describe both Radio-Frequency (RF) and digital hierarchical beam forming approaches.Implementation of both RF and digital beam forming systems on two antenna array demonstrators, namely the electronic multi beam radio astronomy concept and the dual polarization all-digital array. This paper compares and contrast both digital and analogue implementations without considering the deep system design of these arrays. This is the ideal approach for beam forming since. However, the implementation is complicated in the analogue domain and few phase steps will limit resolution, which will also introduce errors in the final beam. Furthermore, to implement multiple beams with an analogue implementation simply multiplies the amount of hardware required for every beam, resulting a complex system. In the digital domain, after digitizing the signal introduces delays which are a multiple of the sample time and simply buffer the signals from elements which require a delay. Higher time resolution, however, is required than just the sample time. This can be achieved by interpolating between two or more samples. There is some complexity involved but it is eminently achievable.

[4] Grady Giles, Jing Wang, Anuja Sehgal, Kedarnath J. Balakrishnan, and James Wingfield in 2008 proposed "Test Access Mechanism for Multiple Identical Cores" A new test access mechanism (TAM) for multiple identical embedded cores is proposed. It exploits the identical nature of the cores and modular pipelined circuitry to provide scalable and flexible capabilities to make trade-offs between test time and diagnosis over the manufacturing maturity cycle from low-yield initial production to high-yield, high-volume production. The test throughput gains of various configurations of this TAM are analyzed. The proposed TAM architecture can easily be extended to utilize the availability of the liberated output channels for multiple tracks of inter-core compare. If the output compaction ratio is chosen to be twice that of the input compression ratio, only half as many out-put channels are required. The architecture is modular and scalable in timing and area and easily works for a large number of cores in SoCs. Test generation complexity of the SoC is also reduced since core level patterns can be generated and reused for the different cores. The protocol translation transforms re-quired to convert the core-level patterns to SoC patterns.

3. PROPOSED SYSTEM

Proposed system is to design a multi core parallel testing architecture using majority logic technique. This technique is used to test the all internal core architecture for parallel form.

This work is to implement the test pattern creation and to apply the scan chain process. This process is to analysis the separate core internal architecture output result values. Proposed system is to modify the majority selection process and fault identification comparison process between expected test response and present test response results. The proposed test scheme sharing free variables in common test channels. The cores using the exact same TAM lines are divided into a group. Cores in the same group are tested sequentially unless their test patterns are compatible. Those using not identical TAM lines (in the different groups) can be tested in parallel. Compressed test data is delivered from tester via TAM and decompressed in the cores by linear decompressor. Then the decompressed test patterns are scanned into scan chains in cores. During test, if two cores in the different groups have some common TAM lines then the free variables delivered by the common TAM lines can be shared by these cores. When decompressing a test cube for a core in group one/two, if there exist more free variables transported in the common TAM than necessary, then test cubes for other cores in group two/one can be decompressed using these variables. To guarantee that test cubes for two cores tested simultaneously can be encoded successfully, the use for free variables in common test channels must be limited. These test cubes should be chosen under the constrains that there exist enough free variables to solve successfully the system of linear equations corresponding to all specified bits. The specified rate of test cubes for a core varies considerably, so the requirements to test channels are obviously different. The number of common channels concerns the compression efficiency in the test scheme. If the proportion of common channels for the core is too high, maybe no test cube of the core can be encoded successfully when other core are tested with test cubes containing many specified bits. Conversely, low proportion of common channels for the cores tested simultaneously may reduce compression efficiency in the SoC test scheme. A generic test communication protocol is proposed, which can be applied to regular SoC topologies. In this protocol, test patterns, coming from the external tester, are simultaneously applied to all identical routers. Test responses of the routersare internally compared. If test responses are different, a mechanism for diagnosis can be activated. Otherwise, the test continues.

Fig 1 shows the flow diagram that a single scan chain per router is assumed and the four chains feed the single comparator. Ideally, all routers are tested in parallel and a single comparator is used. The SoC designer can define an alternative solution by increasing the number of scan chains per router to reduce test time and increasing the number of comparators, whose area can be easily estimated. While the broadcast-based TAM compares the response data to the expected data in the chip, the majority-based TAM compares the response data to the majority data in the chip.

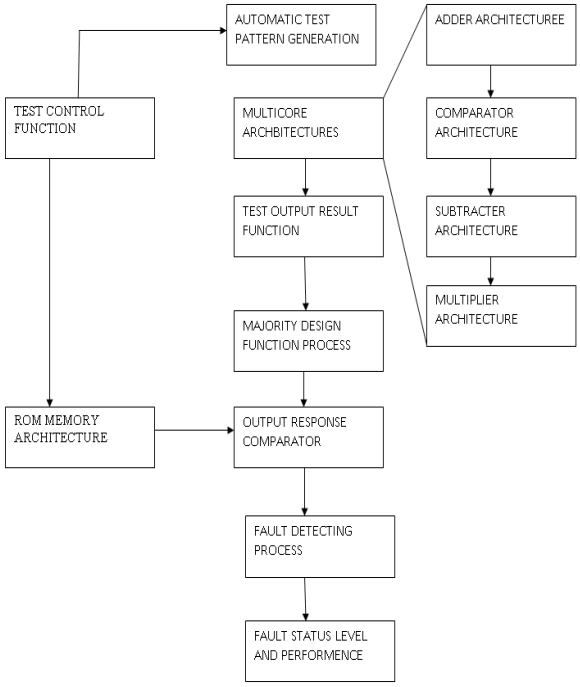

Fig 1: Flow diagram

For an example, each core has two scan chains, so TDI and TDO each require two test pins. Majority analyzer (MA) 1 represents the MA module for Scan chain 1 of each core; its output is connected to the first pin of TDO. The MA is a bit-wise architecture and the test responses of Scan chain 1 from every core are compared with the output of MA 1 by XOR gates. If any of the test response data in a scan chain differ from the majority data, the core producing the different data is regarded as a faulty core and is recorded in that core's E register. During the test process, if the ATE confirms that the TDO differs from the expected data, this means that more than half the cores have faults and thus the multicore system under test will be discarded. On the other hand, if there are no differences between the TDO and the expected data throughout the test process, this means that the multicore system can be salvaged and used. Otherwise, this test process is repeated until all the test patterns have been used, and if the test process ends without any of the majority values differing from the expected test data, the ATE then reads the error registers. The majority-based TAM is only related to the delivery of test response data and it can be compatible and improved with the existing DFT technologies.

4. RESULT

The simulation result of BIST architecture based on multicore test is shown in fig 2.

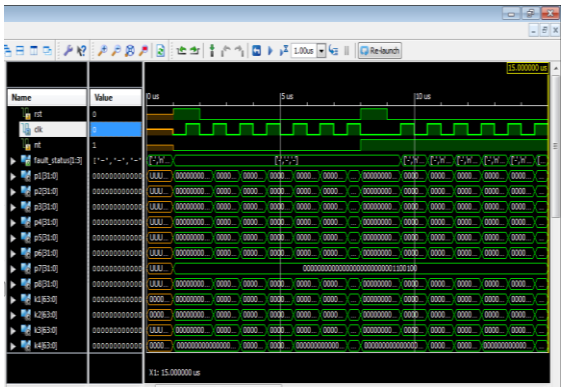

Fig 2: Simulation result of multicore based BIST architecture

5. CONCLUSION

The low-power scan chain based parallel multi core testing architecture is designed. This architecture consists of different core architecture and to identify the faulty circuit using majority logic technique. By sharing free variables between cores tested simultaneously in SOC, the proposed SOC test technique provides greater flexibility in test compression. It does not have effects on an additional area and potential performance overhead. Experimental results on several larger SOC designs demonstrate the efficiency of the proposed technique. The proposed scheme can also be expanded by sharing common channels among three or more core groups to obtain better results. Meanwhile, the proposed approach can be combined with other approaches, such as test scheduling, to reach higher efficiency.

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